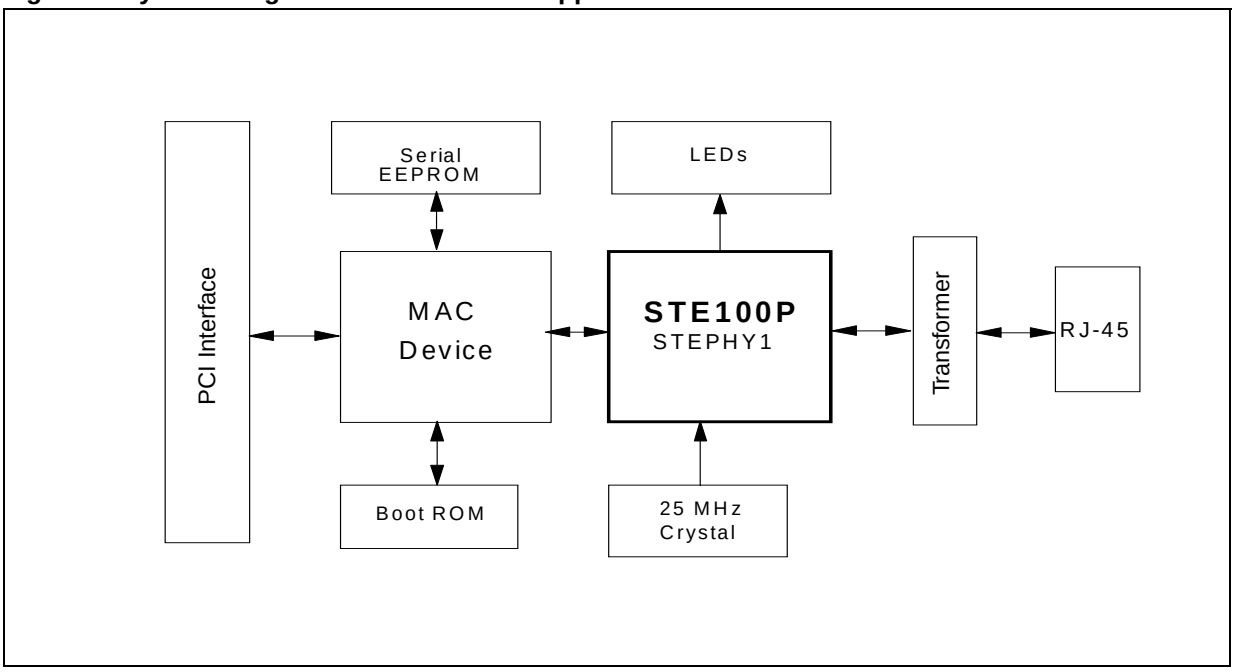
STE100P - SINGLE PORT FAST ETHERNET TRANSCEIVER

1.0 GENERAL DESCRIPTION

The STE100P, also referred to as STEPHY1, is a high performance Fast Ethernet physical layer interface for 10BASE-T and 100BASE-TX applications. It was designed with advanced CMOS technology to provide a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MAC) and a physical media interface for 100BASE-TX and 10BASE-T. The twisted pair interface directly drives a 10/100 twisted pair connection. STE100P is an excellent device perfectly suited for hub, switch, router and other embedded Ethernet applications.

The system diagram is as shown below:

Figure 1. System Diagram of the STE100P Application



2.0 FEATURES

- Integrates the whole physical layer functions of the 100BASE-TX and 10BASE-T
- 3.3V low power operation
- The hardware control pins set the initial state of the STE100P at power-up
- Designed with a power down feature, which can save the power consumption significantly
- Can operate for either full duplex or half duplex network applications.
- MII interface
- Provides auto-negotiation, parallel detection or manual control for mode setting
- Provides MLT-3 transceiver with DC restoration for Base-line wander compensation

- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides loop-back modes for diagnostic testing
- Builds in Stream Cipher Scrambler/Descrambler and 4B/5B encoder/decoder
- Supports external transmit transformer with turn ratio 1:1
- Supports external receive transformer with turn ratio 1:1

3.0 DESIGN AND LAYOUT GUIDELINES

3.1 General Guidelines

- Verify that all components meet application requirements.
- Design in filters for the analog power circuits.
- Use bulk capacitors (10-22uF) between the power and ground planes to minimize switching noise, particularly near high-speed busses (>25 MHz).
- Use an ample supply of 0.1uF decoupling capacitors to reduce high-frequency noise on the power and ground planes.
- Use a single analog power and ground plane for multiple devices. Keep ferrite bead currents under 65% of the rated load
- Avoid breaks in the ground plane, especially in areas where it is shielding high-frequency signals.
- Keep power and ground noise levels below 50mV
- Keep high-speed signals out of the area between STE100P and the magnetics
- Ensure that the power supply is rated for the load and that output ripple is minimal (<50mV)
- Route high-speed signals next to a continuous, unbroken ground plane.
- Provide impedance matching on long traces to prevent reflections.
- Do not route any digital signals between the STE100P and the RJ-45 connectors at the edge of the board
- It is recommended to fill in unused areas of the signal planes with solid copper and attach them with vias to a Vcc or ground plane that is not located adjacent to the signal layer.

3.2 Differential Signal Layout Guidelines

- Route differential pairs close together and away from everything else
- Keep both traces of each differential pair as close to the same length as possible.
- Avoid vias and layer changes
- Keep transmit and receive pairs away from each other. Run orthogonally, or separate with a ground plane layer.

3.3 Power and Ground

In order to obtain high speed communications design, the power and ground planes may be conceptually divided into three regions (the analog and digital power planes and the signal ground plane)

The analog power region extends from the magnetics back to the STE100P, whereas the digital power region extends from the MII interfaces of the STE100P through the rest of the board. Only components and signals pertaining to the particular interface should be placed or routed through each respective region. The digital section supplies power to the digital Vcce/i pin and to the external components. The analog section supplies power to Vcca pins of the STE100P.

The signal ground region is one continuous, unbroken plane that extends from the magnetics through the rest

of the board. The signal ground plane may be combined with chassis ground or isolated from it. If the ground planes are combined, an isolation area is not required. When laying out ground planes, special care must be taken to avoid creating loop antenna effect. Some guidelines are as follows-

- Run all ground plane as solid square or rectangular regions
- Avoid creating loops with ground planes around other planes

3.4 Recommendations

The following recommendations apply to design and layout of the power and ground planes and will prevent the most common signal and noise issues.

- Divide the Vcc plane into two sections - analog and digital. The break between the planes should run under the device.
- When dividing the Vcc plane, it is not necessary to add extra layers to the board. Simply crate moats or cutout regions in existing layers.
- Place a high-frequency bypass cap (0.1uF) near each analog Vcc pin
- Join the digital and analog sections at one or more points by ferric beads. Ensure that the maximum current rating of the bead is at least 150% of the nominal current that is expected to flow through it. (250mA per STE100P)
- Place a bulk capacitor (22uF) on each side of each ferrite bead to stop switching noise from travelling through the ferrite.

For designs with multiple STE100P's, it is acceptable to supply all from one analog Vcc plane. This plane can be joined to the digital Vcc plane at multiple points, with a ferrite bead at each one.

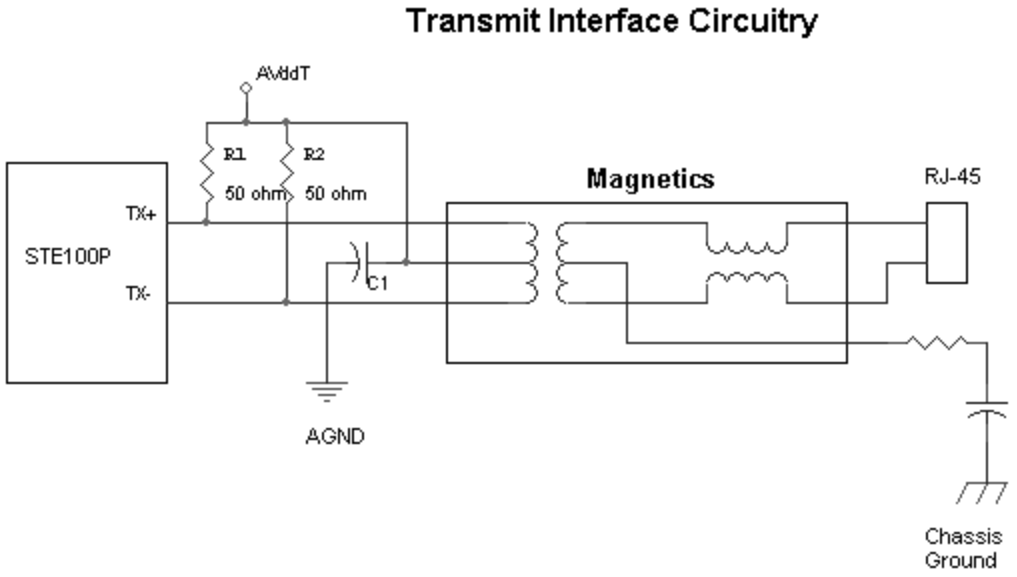
4.0 TWISTED PAIR INTERFACE

4.1 Transmit Interface Circuitry

Figure 2 shows a typical transmit interface circuitry. Current is sourced by the AVddt output to the centertap of the primary side of the winding. Current flows from the centertap to TX+ and TX-. Other components are as follows:

- R1 and R2 are 49.9 ohm resistors that provide impedance matching to the line, which has a nominal impedance of 100 ohm.
- C1 shunts any common-mode energy present in the output to ground.
- The magnetics consists of the main winding and a common-mode choke.
- The common-mode choke stops common mode energy from reaching the line. It works together with capacitor C1 to direct common-mode energy away from the line.

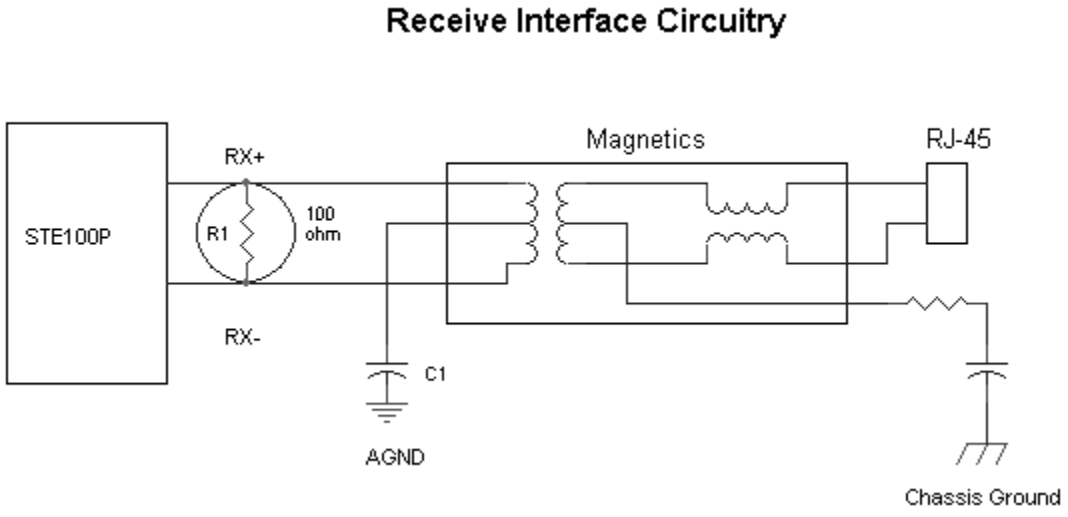
Figure 2. Transmit Interface Circuitry



4.2 Receive Termination Circuitry

The receive termination circuit as shown in Figure 3 is a simple 100 ohm, 1% resistor across the RX+/ RX- pair. The receive circuit consists of magnetics, which include a main winding and a common-mode choke, and termination resistance to match the line impedance. The common-mode choke can be located on either the primary or secondary side of the winding. Some vendors place the receive common-mode choke on the line-side (primary) of the main winding while others place it on the device side (secondary). Either location is acceptable.

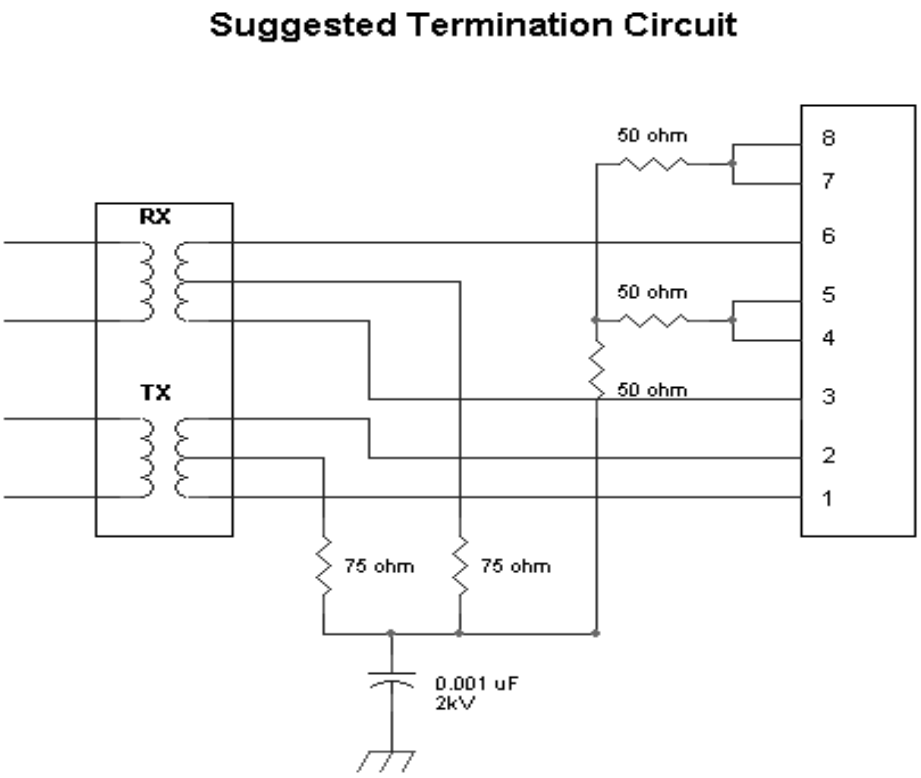
Figure 3. Receive Interface Circuitry



4.3 Standard termination

ST recommends a standard termination for the unused pairs on the twisted-pair interface as shown in Figure 4. The termination basically looks like a 100 ohm load, matched to the line, which is by passed to chassis ground. This termination is added for robustness and noise reduction.

Figure 4. Suggested Termination Circuit



5.0 CRYSTAL REQUIREMENTS

The crystal to be used with the STE101P should be a 25 MHz fundamental mode crystal operating in parallel resonance, connected as shown in the sample application circuit schematic (see section 7.1). The following table shows the specifications for the crystal:

Parameter	Units	Min	Max	Nom
Frequency	MHz	-	-	25.0
Frequency Stability	ppm	-	± 50	-
Load Capacitance	pF			18
Shunt Capacitance	pF		8	

Table 1

6.0 LED PINS

The LED display, consists of five LEDs having the following characteristics:

- Speed LED: 100Mbps(on) or 10Mbps(off)
- Transmit/Receive LED: Blinks at 10Hz when transmitting or receiving, but not colliding
- 10Mbps LED: Blinks at 10Hz when transmitting, but not colliding
- Link LED: On when 100M or 10M link ok
- Collision/FD LED: Blinks at 20Hz to indicate a collision. On to indicate full duplex operation

7.0 TYPICAL APPLICATION

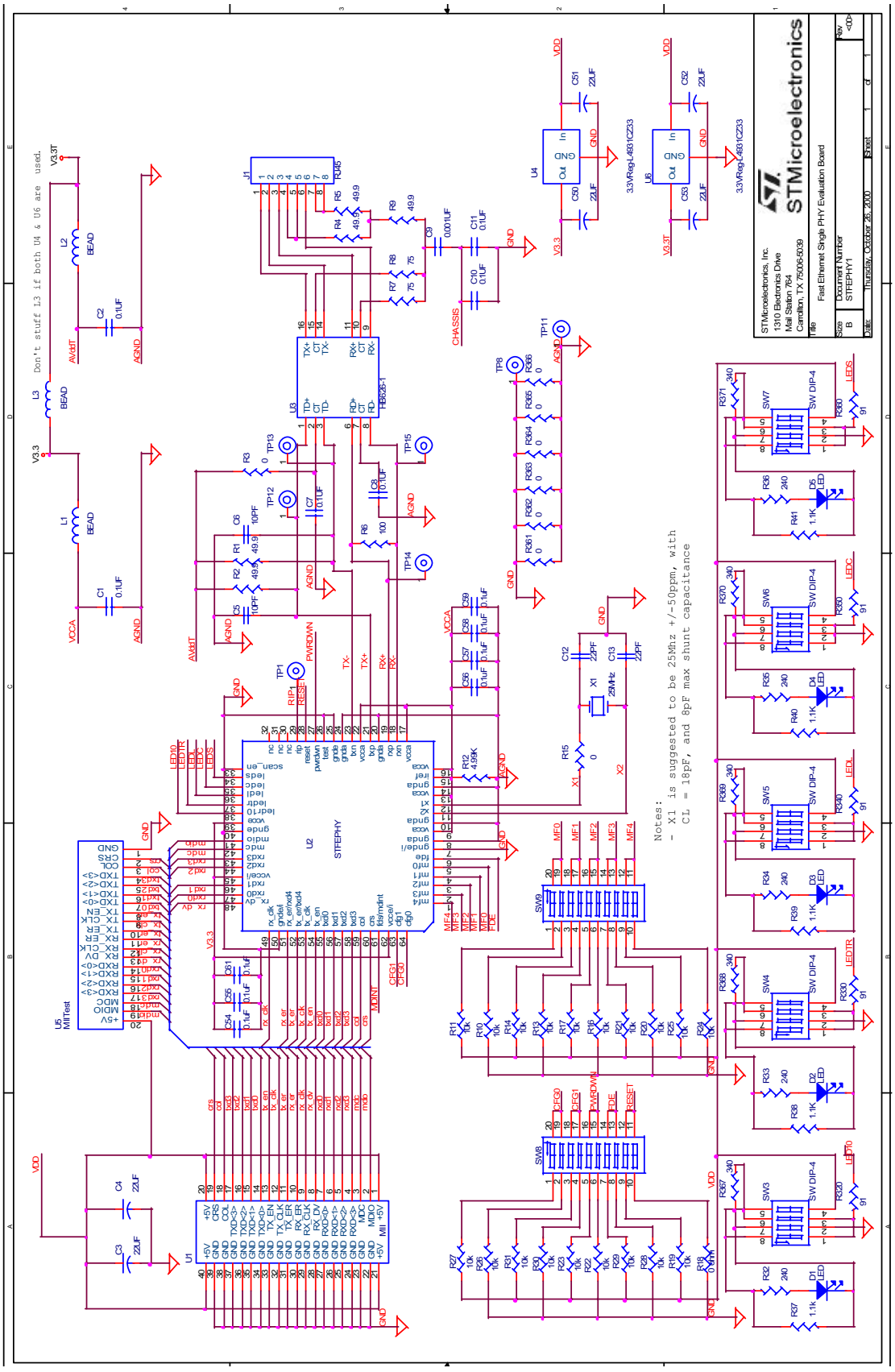
While the STE100P may be used in a variety of applications such as multi-port repeaters or switches, the application shown below gives a very simple way of evaluating and using the STE100P with minimum circuitry. (Refer to Bill of Materials in Table 2)
A typical application of the STE100P presented here would be in designing a Fast Ethernet transceiver with a standard MII interface and a 10/100 Mbps twisted pair connector. (Refer to Fig. 5)
In this application,

- STE100P is the only IC needed.
- It connects directly to the industry standard 40-pin MII connector.
- It also connects to the RJ-45 jack via a standard Fast Ethernet transformer.
- 5, 4-position DIP switches are used to select the PHY address. (More details on the PHY address registers, etc. are available on the STE100P datasheet)
- 2, 10-position DIP switches are used for determination of all of the pin-selectable options of the STE100P such as duplex mode, data rate and auto negotiation.
- STE100P also supports the MII MDIO access to all of its internal registers.
- LEDs are included to indicate status information such as speed, duplex mode, transmit and receive activity and link status.
- There are registers with 16 bits each supported for STE100P. (More details on these registers are available in the STE100P datasheet).
- There are also 4 special registers for advanced chip control and status information.

7.1 Schematics

The schematics for the sample application can be found on the the following page and the ST website at:

http://www.st.com/prodpres/dedicate/telecom/network/datacom/st100p.htm


STMicroelectronics
STMicroelectronics, Inc.
1310 Electronics Drive
Mail Station 764
Carrollton, TX 75006-5039
Title
Fast Ethernet Single PHY Evaluation Board
Size
B
Document Number
STFEPHY1
Rev
<00>
Date:
Thursday, October 26, 2000
Sheet
1
of
1
Don't stuff L3 if both U4 & U6 are used.
Notes:
- X1 is suggested to be 25Mhz +/-50ppm, with
CL = 18pF, and 8pF max shunt capacitance
STFEPHY
MiiTest

7.2 Bill of Materials

Following are the Bill of Materials for the STE100P sample application.

Item	Qty	Reference	Part
1	13	C1,C2,C7,C8,C10,C11,C54, C55,C56,C57,C58,C59,C61	0.1uF
2	6	C3,C4,C50,C51,C52,C53	22UF
3	2	C5,C6	10PF
4	1	C9	0.001UF
5	2	C12,C13	22PF
6	5	D1,D2,D3,D4,D5	LED
7	1	J1	RJ45
8	3	L1,L2,L3	BEAD (do not install L3 if U4 & U6 both installed)
9	5	R1,R2,R4,R5,R9	49.9
10	8	R3,R15,R361,R362,R363, R364,R365,R366	0 ohm
11	1	R6	100 ohms
12	2	R8,R7	75 ohms
13	19	R10,R11,R13,R14,R16,R17, R19,R20,R21,R22,R23,R24, R25,R26,R27,R28,R29,R30, R31	10k
14	1	R12	4.99K
15	1	R18	0 ohm
16	5	R32,R33,R34,R35,R36	240 ohms
17	5	R37,R38,R39,R40,R41	1.1K
18	5	R320,R330,R340,R350,R360	91 ohms
19	5	R367,R368,R369,R370,R371	340 ohms
20	5	SW3,SW4,SW5,SW6,SW7	DIP Switch DIP-4
21	2	SW8,SW9	SW DIP-10
22	7	TP1,TP8,TP11,TP12,TP13, TP14,TP15	Test Pins
23	1	U1	MII 40 pin connector
24	1	U2	STEPHY STE100P
25	1	U3	HB626-1 Transformer
26	2	U4,U6	3.3VReg-L4931CZ33
27	1	U5	MIITest header
28	1	X1	25MHz crystal

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